

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : To Be Assigned  
Applicant(s) : KONDO, Masayoshi et al.  
Filed : Concurrent Herewith  
TC/A.U. : To Be Assigned  
Examiner : To Be Assigned  
Title : Circuit Boards, Multilayer Wiring Boards, Method of Producing Circuit Boards, and Method of Producing Multilayer Wiring Boards

Confirmation No. TBA

Docket No. : 033036.088  
Customer No. : 25461

Mail Stop PCT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
Attn: DO/EO/US

Sir:

**INFORMATION DISCLOSURE STATEMENT**

Pursuant to the duty of disclosure under 37 C.F.R. 1.56, Applicants are enclosing an Information Disclosure Statement by Applicant (Form PTO/SB/08a) and copies of the foreign patent documents cited therein. The relevance of the cited documents is indicated in the International Search Report, dated February 24, 2004, being submitted herewith.

It is respectfully requested that the cited documents be considered by the Examiner in the above-identified patent application and that the cited documents be made officially of record therein. It is further requested that a listing of the same appear on the face of any patent which may issue from this application.

A first Official Action has not yet issued for this application. Therefore, it is believed that no fees are due under 37 C.F.R. Section 1.97(b)(3).

Respectfully submitted,



By: Robert G. Weilacher, Reg. No. 20,531

Dated: May 16, 2005  
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To Be Assigned **10/534962**

Application Number

**Filing Date**

**First Named Inventor**

**Art Unit**

**Examiner Name**

Attorney Docket Number

**Concurrent Herewith**

KONDO, Masayoshi et al.

## To Be Assigned

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[illegible][illegible]

Date Considered

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Translation is attached.

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